What is claimed is:

1. A semiconductor imaging chip comprising:

an array of active pixel sensors arranged in rows and columns;

an output terminal; and

a multiplexed column buffer having a plurality of input terminals coupled to a respective plurality of said columns and a multiplexed column buffer output terminal coupled to said output terminal.

2. A semiconductor imaging chip in accordance with claim 1, wherein said multiplexed column buffer further comprises a multiplexed differential gain amplifier.

3. A semiconductor imaging chip in accordance with claim 1, wherein said multiplexed column buffer further comprises a multiplexed bus driver amplifier.

4. In a semiconductor imaging chip having an array of active pixel sensors arranged in rows and columns, a multiplexed column buffer comprising:

respective first and second memory elements;

respective first, second, third, and fourth switches;

a differential gain amplifier;

said first switch coupling said first memory element to a first column of said array of active pixel sensors;

said second switch coupling said second memory element to a second column of said array of active pixel sensors;

said third switch coupling said differential gain amplifier to said first memory element; and

said fourth switch coupling said differential gain amplifier to said second memory element.

5. In a semiconductor imaging chip having an array of active pixel sensors arranged in rows and columns, and an output bus terminal, a multiplexed column buffer comprising:

respective first and second memory elements;

respective first and second switches;

a bus driver amplifier having respective input and output terminals;

said first memory element being coupled to a first column of said array of active pixel sensors;

said second memory element being coupled to a second column of said array of active pixel sensors;

said first switch coupling said first memory element to said input terminal of said bus driver amplifier;

said second switch coupling said second memory element to said input terminal of said bus driver amplifier; and

said output terminal of said bus driver amplifier being coupled to said output bus terminal of said semiconductor imaging chip.

6. A multiplexed column buffer in accordance with claim 5, wherein said first memory element is coupled to said first column of said array of active pixel sensors and said second memory element is coupled to said second column of said array of active pixel sensors through a differential gain amplifier.

7. A multiplexed column buffer for use in a semiconductor imaging chip including an array of active pixel sensors arranged in rows and columns, said semiconductor imaging chip having an output terminal, said multiplexed column buffer comprising:

respective first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth memory elements;

respective first, second, third, fourth, fifth and sixth switches;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

a bus driver amplifier having respective input and output terminals;

said first switch coupling said first memory element to a first column of said array of active pixel sensors;

said second switch coupling said second memory element to the said first column of said array of active pixel sensors;

said third switch coupling said third memory element to said second column of said array of active pixel sensors;

said fourth switch coupling said fourth memory element to said second column of said array of active pixel sensors;

said fifth switch coupling said first memory element to said first input terminal of said differential gain amplifier;

said sixth switch coupling said third memory element to said first input terminal of said differential gain amplifier;

said seventh switch coupling said second memory element to said second input terminal of said differential gain amplifier;

said eighth switch coupling said fourth memory element to said second input terminal of said differential gain amplifier;

said ninth switch coupling said fifth memory element to said output terminal of said differential gain amplifier;

said tenth switch coupling said sixth memory element to said output terminal of said differential gain amplifier;

said eleventh switch coupling said fifth memory element to said input terminal of said bus driver amplifier;

said twelfth switch coupling said sixth memory element to said input terminal of said bus driver amplifier; and

said output terminal of said bus driver amplifier being coupled to said output terminal of said semiconductor imaging chip.

8. In a semiconductor imaging chip having an array of active pixel sensors arranged in rows and columns, said semiconductor imaging chip including at least one differential gain amplifier, a multiplexed readout method comprising:

storing a first APS pixel signal value from a first column of said array of active pixel sensors to form a stored first APS pixel signal value;

storing a second APS pixel signal value from a second column of said array of active pixel sensors to form a stored second APS pixel signal value;

coupling said stored first APS pixel signal value to said differential gain amplifier; and

coupling said stored second APS pixel signal value to said differential gain amplifier.

9. In a semiconductor imaging chip having an array of active pixel sensors arranged in rows and columns, said semiconductor imaging chip including a pattern cancellation circuit for providing a corrected APS pixel signal value, said semiconductor imaging chip further including at least one bus driver amplifier, and output bus terminal, a multiplexed readout method comprising:

storing a first corrected APS pixel signal value;

storing a second corrected APS pixel signal value;

coupling said stored first corrected APS pixel signal value to said bus driver amplifier; and

coupling said stored second corrected APS signal value to said bus driver amplifier.

10. A semiconductor imaging chip comprising:

an array of active pixel sensors arranged in rows and columns;

an output terminal; and

a multiplexed column buffer having a plurality of input terminals and a respective output terminal, said multiplexed column buffer further including a differential gain amplifier selectively connected to at least two of said plurality of input terminals so as to be multiplexed among at least two of said columns; wherein

said plurality of input terminals of said multiplexed column buffer is respectively coupled to said plurality of said columns and said multiplexed column buffer output terminal is coupled to said output terminal.

11. A semiconductor imaging chip in accordance with claim 10, wherein said multiplexed column buffer further comprises a multiplexed bus driver amplifier.